5

Our Case No. 10808/117

10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES LETTERS PATENT

INVENTORS: JOERG WOHLFAHRT
THOMAS HLADSCHIK
JENS HOLZHAEUSER
DIETER RATHEI

TITLE: METHOD OF AND SYSTEM FOR
ANALYZING CELLS OF A MEMORY
DEVICE

ATTORNEY: JOHN J. KING
BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

METHOD OF AND SYSTEM FOR
ANALYZING CELLS OF A MEMORY DEVICE

FIELD OF THE INVENTION

[0001] The present invention relates generally to memory devices, and in particular, to a method of and system for analyzing cells of a memory device.

BACKGROUND OF THE INVENTION

[0002] In a memory device, such as a dynamic random access memory (DRAM), information is stored in capacitors accessed via a transistor (i.e. transfer gate). The two different states this capacitor (i.e. charged or discharged) can be set to corresponding to the two different pieces of information needed in digital algebra, "true" and "false". A variety of leakage currents may lead to a loss of information by discharging this capacitor without access being controlled. In order to take the proper corrective steps to improve the manufacturing process of the device, it may be beneficial to identify the primary causes of the leakage. It may be beneficial to distinguish between leakage related to failing cells (i.e. "soft fails") from other failing cells (i.e. "hard fails") in order to determine the appropriate corrective actions.

[0003] A standard DRAM design uses a wordline (WL)/bitline (BL) architecture, where a DRAM storage cell is addressed by a specific WL and a BL address. Process faults lead to failures in wordlines and/or bitlines, causing complete and/or partial WL and/or BL fails and/or other fail patterns like single cells, paired cells, etc.. Fails in a very early state of WL/BL address decoding hierarchy of course lead to multiple WL or BL failures or even to failures of large memory cell blocks. Due to redundancy

1

limitations, block fails may not be repairable, although sparse fails (WL, BL and single cell fails) can be repaired if not too densely packed.

[0004] Because of the reverse biased junction between a capacitor and p-well of the transfer device, a reverse current or junction leakage will decrease the amount of charge stored in the capacitor over time. In order to get correct results of a READ operation, the information stored in the capacitor cell has to be refreshed periodically. Leakage current and refresh intervals are synchronized so that the information stored will not dissipate, unless additional leakage will disturb this synchronization leading to soft fails. Typically, partial WL or BL fails turn into full WL or BL fails over time. In addition to the filled up WL and BL fails, some weak single cells (SC) and paired cells (PC) will start to fail with a longer time between the refresh cycles.

[0005] Because partial WL fails need to be repaired with a redundant WL element, the repair of the entire WL comes at no additional costs of redundant cells. However, unlike those fails of a partial WL or BL or a full WL or BL, single cell or paired cell fails are randomly distributed across the memory cell array and require one redundancy array (RA) element for each fail. Such single cell or paired cell fails can make it difficult to repair a cell, and therefore such information can be critical in determining whether a cell can be repaired.

[0006] Accordingly, there is a need for an improved system and method of analyzing cells of a memory device.

SUMMARY OF THE INVENTION

[0007]   A method of analyzing cells of a memory device is disclosed. The method allows a non destructive, automized analysis of the prevailing leakage mechanisms in memory cells such, as DRAMs. Hence, main data retention yield detractors can be identified and corrective process actions can be taken. Since the method is used at wafer level and is non destructive, components can be built and their behaviour in burn-in, early life tests etc. can be observed.

[0008]   The method generally comprises steps of establishing a plurality of fail signatures, wherein each fail signature is associated with a type of failure. Voltages according to a plurality of test patterns are applied to nodes of a cell of the memory device. Fail data of the cell for the plurality of patterns is then analyzed, and a fail signature of the cell is determined. A type of failure of the cell is then determined based upon the plurality of fail signatures.

[0009]   A system for analyzing cells of a memory device is also disclosed. The system preferably comprises a plurality of probes applying test voltages to a cell of the memory device. A control circuit varies the voltages applied to the cell, and analyzes the failures of the cell as the voltages applied to the cell are varied. Finally, an output device generates an output indicating a type of failure of the cell.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010]   Fig. 1 is a block diagram of a system for analyzing cells of a memory device according to the present invention;

3

[0011]   Fig. 2 is a block diagram of a dynamic random access memory according to the present invention;

[0012]   Fig. 3 is a circuit diagram of a cell of the dynamic random access memory of Fig. 2;

[0013]   Fig. 4 is a cross section of a portion of a cell of the dynamic random access memory of Fig. 2;

[0014]   Fig. 5 is a bit fail map of a memory device generated according to a first step of the present invention;

[0015]   Fig. 6 is a bit fail map of a memory device generated according to a second step of the present invention;

[0016]   Fig. 7 is an overlay of bit maps according to the present invention;

[0017]   Fig. 8 is a signature table showing signatures for cells of a particular device during nominal test conditions according to the present invention;

[0018]   Fig. 9 is a signature table showing induced leakage signatures for cells of a particular device according to the present invention;

[0019]   Fig. 10 is a flow chart showing a method of analyzing cells of a memory device according to the present invention;

[0020]   Fig. 11 is a flow chart showing a method of analyzing cells of a memory device according to an alternate embodiment of the present invention; and

[0021]   Fig. 12 is a flow chart showing a method of analyzing cells of a memory device according to a further embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0022]   Turning first to Fig. 1, a block diagram of a system for analyzing cells of a memory device according to the present invention is shown. In particular, a system 100 comprises a computer 102 having a user interface 104 and a display 106, which is coupled to test equipment 108. The test equipment 108 preferably comprises probes 112 which are adapted to provide voltages to nodes of a chip 114 of a wafer 116. The computer 102 is preferably coupled to an output device 118. The output device 118 could be, for example, a printer, a storage device, or some other means for receiving data recorded by the computer 102. The computer 102 could be any device having a control circuit, such as microprocessor or an application specific integrated circuit (ASIC) for enabling the processing of data and the generation of an output, as will be described in more detail reference to the remaining figures. Similarly, test equipment 108 including test fixture 110 could be any type of conventional test equipment for applying voltages to nodes of the integrated circuit. Although an example of a system for analyzing cells of a memory device is shown in Fig. 1, other systems well known in the art could be used to implement the present invention.

[0023]   Turning now to Fig. 2, a block diagram of a dynamic random access memory according to the present invention is shown. In particular, a DRAM 200 comprises an array 202 of cells having a plurality of the bit lines 204 and a plurality of word lines 206. A cell 208, which is formed at the intersection of a word line and a bit line as is well known in the art, is shown in more detail in reference to Figs. 3 and 4. A decoder 210 is coupled to receive a chip select signal and an address, and generates an output to a driver

212. The driver 212 addresses a cell of the chip to read or write data to the DRAM by way of a sense amplifier 214. The method of the present invention enables detecting cells of the DRAM which are failing or leaking, and determine a type of failure for a given cell.

[0024] Turning now to Figs. 3 and 4, a circuit diagram and a cross sectional view of a cell of the dynamic random access memory of Fig. 2 are shown in Figs. 3 and 4, respectively. The standard single device cell of the DRAM consists of a single capacitor located across source and drain of a negatively biased transistor. The schematic of DRAM trench cell with transfer gate preferably has the following default voltages:

V_{BB}	-V1	back bias
V_{PP}	+3.5*V1	wordline boost voltage
V_{BLEQ}	+V1	bitline equalize voltage
V_{BLH}	+2*V1	bitline high voltage
V_{PL}	+V1	plate voltage

[0025] The applied voltages can be externally forced to different values via bond pads. These bond pads are generally available only during wafer test, and therefore they will not be connected to pins of the lead frame. In order to determine which leakage was responsible for a single cell (SC) or a paired cell/ (PC) to fail at data retention (i.e. a certain refresh interval), the internal voltage of the chip can be varied in a way that this leakage will be reduced and the failing cell will pass. However, this variation suppressing one leakage mechanism can induce other leakage currents making the cell fail again. Based upon an understanding of the cells of the chip and through

experimentation, failure signatures for a cell of a given device can be developed. As will

be described in more detail in reference to remaining figures, a series of voltage patterns

are applied and the failure pattern for a cell is analyzed to determine the type of failure.

[0026] Turning now to Fig. 4, a cross section of a portion of a cell of the dynamic

random access memory of Fig. 2, and identifying various nodes of the schematic diagram

of Fig. 3, is shown. In particular, a substrate 402 has a p-well 404 and a plurality of n-

poly trenches 406. A word line 408 (comprising the V_{PP} node) and a word line 410 (both

of which extend in the z-direction) are formed over the p-well, while a bit line 412

extends over the word lines including word line 410 and additional word lines 420. A

V_{PL} node 416 and a V_{BLH} node 418 are also shown. As is well known in the art, there are

five main contributors to the total leakage of the cell leading to single cell and paired cell

retention fails, as indicated by the arrows A through E. In particular, arrow A represents

sub V_t leakage. Arrow B represents Buried Strap (BS) junction leakage. Arrow C

represents node dielectric leakage. Arrow D represents gate-induced drain leakage

(GIDL) leakage. Finally, arrow E represents vertical field effect transistor (FET)

leakage. (labels 412 and 420 are never mentioned)

[0027] When identifying which leakage mechanism is dominant in affecting data

retention, determining fail counts is not an effective method. For example, a relatively

small number of randomly distributed single cell fails make a chip not repairable, while

2046 fails of a partially failing WL where the WL has a length of 2048, for example, or

even a fully failing WL do not affect reparability of the cell. That is, a redundant word

line can be used to replace the failing word line. The method of the present invention

distinguishes dangerous SC/PC fails from WL/BL oriented retention fails by making a Bit Fail Map (BFM) related to a data retention test, extracting addresses of WL/BL failures, and counting only those failures that do not have more than one address in one direction in common with a single cell, and counting those with exactly 2 addresses in common with a distance of less than 3 addresses as paired cells.

[0028]   As shown in Fig. 5, a bit fail map of a memory chip, for example a bit fail map of one 1M segment of a 64Mb device 502, generated according to a first step of the present invention is shown. As can be seen in the bit fail map of Fig. 5, the following failed lines or cells exist before removing WL/BL failures:

horizontal: 1 full WL fail 504, 1 partial WL fail 506 extending to a full WL at data detention

vertical: 1 full BL fail 508, 1 partial BL fail 510 extended to a full BL at data retention

random: 2 SC (hard), 4 SC (soft) 512-518.

[0029]   As shown in Fig. 6, bit map of a memory chip generated according to a second step of the present invention (i.e, after removing WL/BL failures) is shown. In particular, the method of the present invention distinguishes dangerous SC/PC fails from WL/BL oriented retention fails by creating an artificial Bit Fail Map (BFM) after data retention test from the stored BFMs, extracting addresses of failures, and counting only those that do not have more than one address in one direction in common as SC and those with exactly 2 addresses in common with a distance of less than 3 addresses as paired

8

cells. A spatial distribution comprising an artificial SC/PC map is created as shown in Fig.6.

[0030] Turning now to Fig. 7, an overlay of bit maps according to the present invention is shown. A combination of several measurements, each performed at different, selectively chosen voltage conditions is needed to distinguish different leakage mechanisms. For each test a bit fail map is stored. At the end of the test sequence, the cumulative failures of all tests are stored as well in a separate bit map. The combination of tests passed and failed is the fail signature of a cell. That is, for each cell (designated cell1 – cell 4), a signature associated with the cell based upon the pass or fail of the cell for a particular test.

[0031] For identifying retention SC/PC fails failing under nominal conditions, one measurement has to be taken under nominal conditions. The artificial SC/PC map (SC map) is created from the cumulative map. The SC map is overlaid with the test maps to identify the root cause for the fails. If the pass/fail signature of the test maps then corresponds to the one particular leakage mechanism, the mechanism is identified. Simple statistics of the different signatures (e.g. counts, chip median/means, wafer median/means, etc) distinguish major and minor effects. The same simple statistics of the induced SC/PC failures lead to a statement about the leakage sensitivity of a product.

[0032] Turning now to Fig. 8, a signature table shows signatures for cells of a particular device during nominal operation according to the present invention is shown. The table is developed based upon analysis of a particular chip by individuals having knowledge of the performance of the chip and through testing. The exemplary data

9

shown in Fig. 8 represents signatures of cell failures of a particular DRAM. However, it should be noted that those signatures are given by way of example, and could be different test conditions or different products. For example, the signature table of Fig. 9 shows induced leakage signatures for cells of a particular device. These leakages are caused by the application of the various patterns of test voltages, but do not indicate a fail cell under nominal conditions.

[0033] Turning now to Fig. 10, a flow chart shows a method of analyzing cells of a memory device according to the present invention. In particular, voltages according to a first test pattern are applied to nodes of a cell of the memory device at a step 1002. Voltages are then applied according to a second test pattern to the nodes of the cell of the memory device at a step 1004. Fail data for the cell of the memory device related to the first test pattern and the second test pattern is then analyzed at a step 1006. A type of failure of the cell based upon the analysis of the fail data is then determined at a step 1008.

[0034] Turning now to Fig. 11, a flow chart shows a method of analyzing cells of a memory device according to an alternate embodiment of the present invention. In particular, a plurality of fail signatures is established at a step 1102. Each fail signature is associated with a type of failure. Voltages according to a plurality of test patterns are then applied to nodes of a cell of the memory device at a step 1104. Fail data of the cell for the plurality of patterns is then analyzed at a step 1106. A fail signature of the cell is then determined at step 1108, and a type of failure of the cell based upon the plurality of fail signatures is determined at a step of 1110.

10

[0035] Turning now to Fig. 12, a flow chart shows a method of analyzing cells of a memory device according to a further embodiment of the present invention. In particular, a plurality of fail signatures for the memory device is established at a step 1202. Each fail signature is associated with a type of failure of a cell. Voltages are applied according to a plurality of test patterns to nodes of a plurality of cells of the memory device at a step 1204. Fail data for the plurality of test patterns applied to the cells at a step 1206. A fail signature of the plurality of cells is determined at a step 1208. The fail signatures of the plurality of cells are compared to the plurality of fail signatures at a step 1210, and a type of failure for each failing cell of the plurality of cells is determined at a step 1212.

[0036] It can therefore be appreciated that the new and novel system and method of analyzing cells of a memory device has been described. The method can be applied to all trench technologies, using the same cell and transistor technology as ES3, SS3, 256M-S17, etc., independent from structural size or chip architecture. It will be appreciated by those skilled in the art that, particular the teaching herein, numerous alternatives and equivalents will be seen to exist which incorporate the disclosed invention. As a result, the invention is not to be limited by the foregoing embodiments, but only by the following claims.

11